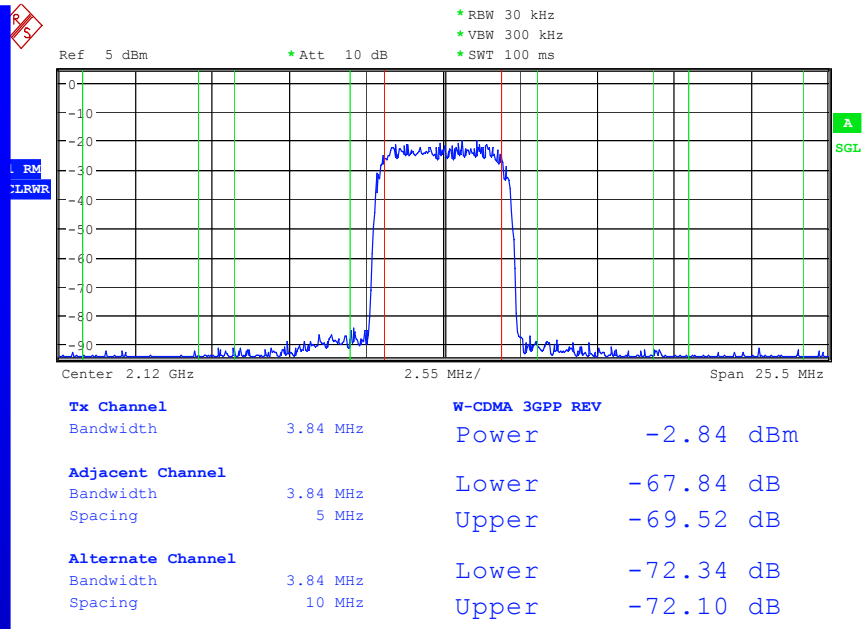

Rohde & Schwarz Products: FSP, FSQ, FSU, FS-K73, SMU200A, SMATE200A, SMJ100A, SMU-K43, SMATE-K43, SMJ-K43, AMIQ, WinIQSIM, CMU200, CMU-K64

High Speed Downlink Packet Access (HSDPA): Challenges for UE Power Amplifier Design

Application Note

This Application Note describes the HSDPA uplink channel structure. Challenges for UE power amplifier design are outlined, and guidelines how to use R&S measurement equipment for testing UE power amplifiers are provided. An outlook on High Speed Uplink Packet Access (HSUPA) and the impact of HSUPA on the uplink channel structure is given.

ROHDE&SCHWARZ

Subject to change – C. Gessner R. Minihold 07.2005 – 1MA84

Contents

The following abbreviations are used in this application note for R&S test equipment:

- The Vector Signal Generator R&S® SMU200A is referred to as the SMU200A.
- The Vector Signal Generator R&S® SMATE200A is referred to as the SMATE200A.
- The Vector Signal Generator R&S® SMJ100A is referred to as the SMJ100A.
- SMU200A, SMATE200A and SMJ100A in general is referred to as the SMx.
- The Vector Signal Generator R&S® SMIQ is referred to as the SMIQ.
- The I/Q Modulation Generator R&S® AMIQ is referred to as the AMIQ.
- The Spectrum Analyzers R&S® FSP and FSU are referred to as FSP and FSU.
- The Signal Analyzer R&S® FSQ is referred to as the FSQ.
- FSP, FSU and FSQ in general is referred to as the FSx.
- The Universal Radio Communication Tester R&S® CMU200 is referred to as the CMU200.

1 Overview

High Speed Downlink Packet Access (HSDPA) is part of 3GPP release 5 of WCDMA. Besides 2 new downlink physical channels for transmission of user data and control information, the **High Speed Dedicated Physical Control Channel (HS-DPCCH)** was introduced as a new **uplink** code channel for control purposes.

The HS-DPCCH puts severe requirements on power amplifier design for HSDPA terminals. Besides being the 3rd uplink code channel, the HS-DPCCH is not continuously transmitted and is not necessarily time aligned with the other WCDMA uplink channels. As a result, varying power relations to the dedicated uplink channels (DPCCH and DPDCH) are obtained.

This Application Note describes the HSDPA uplink channel structure. Challenges for UE power amplifier design are outlined, and guidelines how to use R&S measurement equipment for testing UE power amplifiers are provided. Furthermore, an outlook on High Speed Uplink Packet Access (HSUPA) and the impact of HSUPA on the uplink channel structure is given.

Chapter 2 explains the structure of the HS-DPCCH as well as timing relations and power settings.

Chapter 3 outlines major challenges of the HS-DPCCH channel for UE power amplifier design.

Chapter 4 describes test and measurement requirements relevant for HS-DPCCH as defined in 3GPP.

Chapter 5 explains basic test setups with the help of Rohde & Schwarz measurement equipment. It is explained how to generate and analyze HS-DPCCH signals (manually or with the help of a complimentary demo software).

Chapter 6 exemplarily illustrates HS-DPCCH signal characteristics for different parameter combinations.

Chapter 7 gives an outlook on High Speed Uplink Packet Access.

Chapters 8 to 11 provide additional information including literature references.

This application note assumes basic knowledge of HSDPA technology as outlined in application note 1MA82 [1].

2 Structure of HS-DPCCH

Physical Channel Structure

The HS-DPCCH is an uplink physical channel with fixed spreading factor 256 [2]. It is used to convey user feedback about channel quality (CQI = Channel Quality Indicator) as well as packet acknowledgements or negative acknowledgements (ACK or NACK). No user data is transmitted on the HS-DPCCH.

By using a separate code channel for the HS-DPCCH, backwards compatibility with release 99 is ensured.

The HS-DPCCH is based on a sub-frame structure, with one sub-frame consisting of 3 timeslots (= 2 ms). The packet ACK or NACK information is transmitted in the first timeslot of the sub-frame, and the CQI value is transmitted in the second and third timeslot of the sub-frame.

The structure of the HS-DPCCH is shown in figure 1.

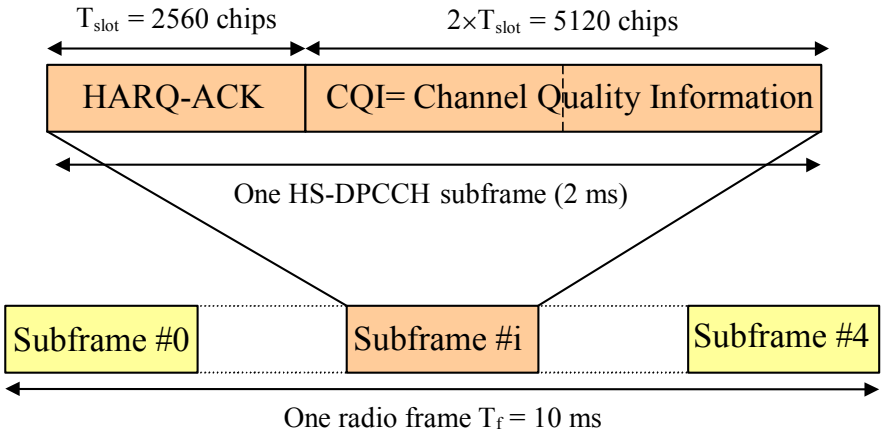

Figure 1 – Structure of HS-DPCCH

The HS-DPCCH is not transmitted continuously. DTX (i.e. no transmission) can occur on ACK/NACK and CQI fields independently from one another. ACK/NACK is only transmitted in case a packet on the downlink HSDPA user data channel (HS-PDSCH, High Speed Physical Downlink Shared Channel) was received by the UE before. CQI is transmitted according to the CQI feedback cycle k parameter which is configured by higher layers, ranging from 0 ms, 2 ms, …, up to 160 ms.

The HS-DPCCH cannot exist as a stand-alone channel, but it always exists together with a Dedicated Physical Control Channel (DPCCH) and possibly one or more Dedicated Physical Data Channels (DPDCH). All these

channels are IQ multiplexed in the uplink [3]. The HS-DPCCH is either mapped on the I domain or on the Q domain, depending on the number of DPDCHs present. If there is an odd number of DPDCHs, the HS-DPCCH is mapped on the Q domain. If there is an even number of DPDCHs, the HS-DPCCH is mapped on the I domain. This is illustrated in figure 2.

The channels are spread individually and scaled by gain factors (see below for more details on gain factor setting).

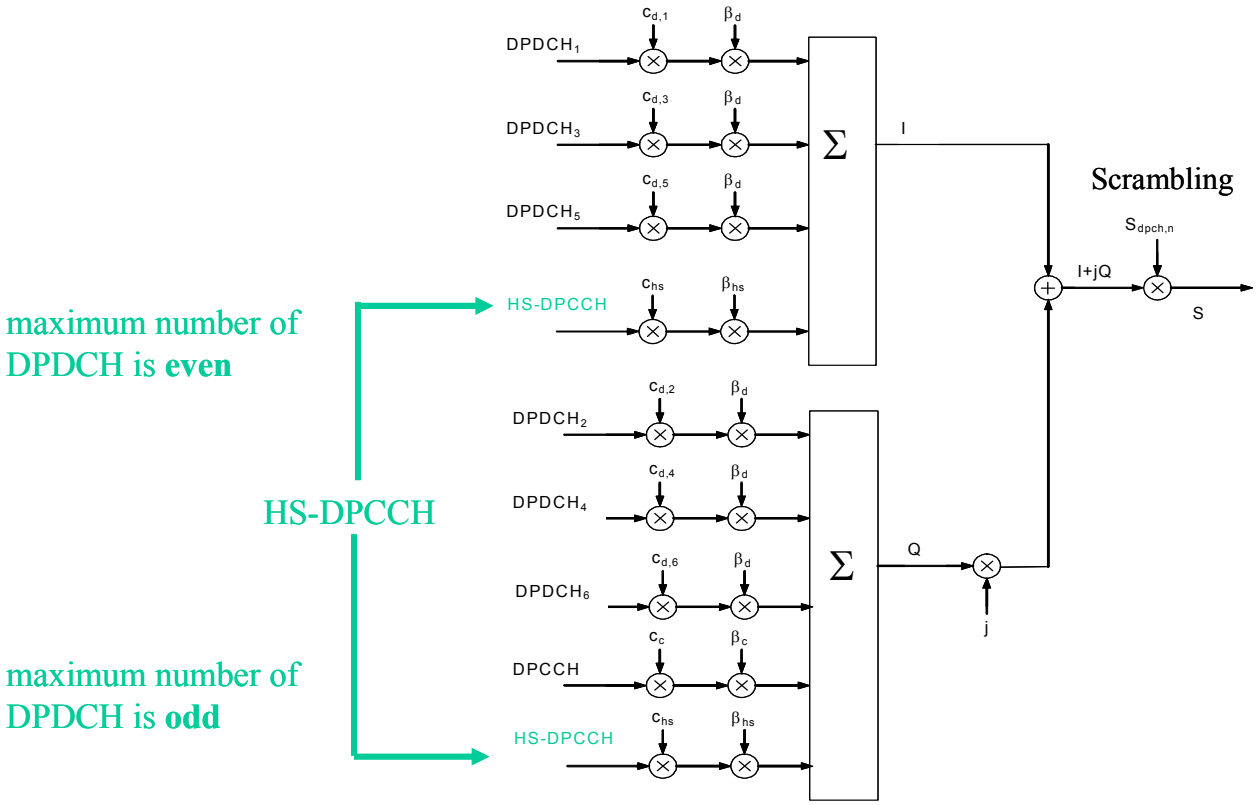

Figure 2 – Spreading for Uplink DPCCH, DPDCHs and HS-DPCCH

Timing Relations

The HS-DPCCH is not necessarily slot aligned with the uplink DPCH.

In order to understand the timing of the HS-DPCCH, it is important to remember the timing relations of the HSDPA related channels in the downlink, High Speed Shared Control Channel (HS-SCCH) and High Speed Physical Downlink Shared Channel (HS-PDSCH). This is because the HS-DPCCH carries the ACK/NACK response for a packet with user data received within an HS-PDSCH sub-frame. Therefore, the timing of the HS-PDSCH directly influences the timing of the HS-DPCCH.

The start of the HS-SCCH which carries scheduling information for HS-PDSCH is aligned with the start of the P-CCPCH frames. The HS-PDSCH

sub-frame associated to an HS-SCCH sub-frame starts $\tau_{HS\text{-}PDSCH} = 2 \times T_{slot} =$ 5120 chips after the start of this HS-SCCH sub-frame, see figure 3.

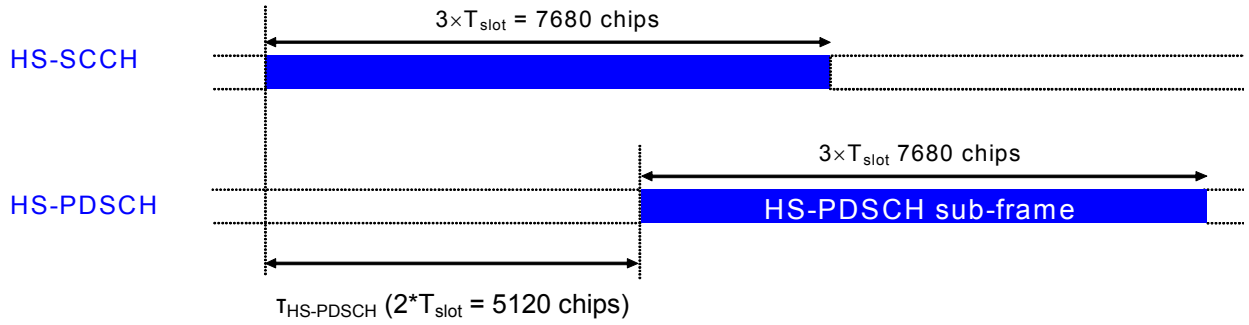

Figure 3 - Timing relation between the HS-SCCH and the associated HS-PDSCH

The downlink DPCH timing may be offset from the P-CCPCH frame timing with a multiple of 256 chips (T_dpch_offset), which is signaled by higher layers to the UE.

All downlink channels are received at the UE with a propagation delay. The UE has to decode the received HS-PDSCH packet and prepare an ACK or NACK for transmission on the HS-DPCCH. For this processing, 7.5 slots corresponding to 19200 chips are assumed as required processing time in the UE (figure 4).

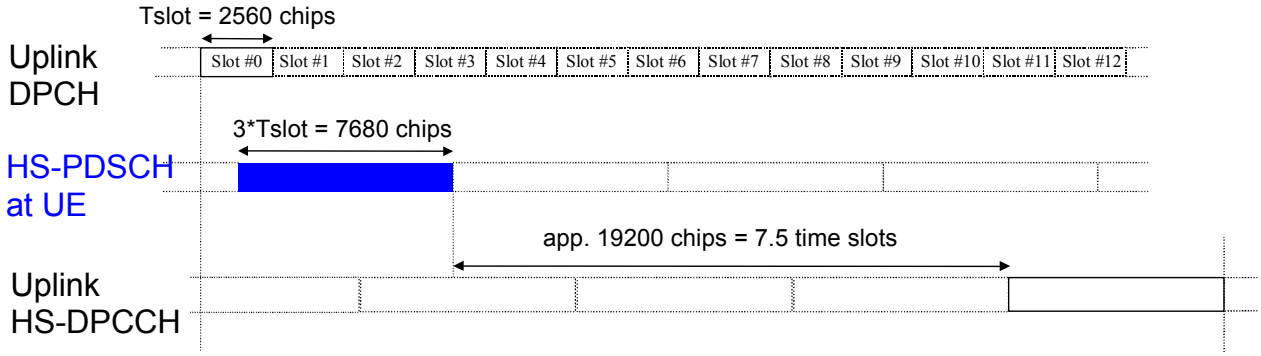

Figure 4 - Timing structure at the UE for HS-DPCCH control signaling

Figure 5 shows the resulting overall timing. The upper part of the figure shows the timing of the downlink channels at the Node B side. The lower part of the figure shows the timing at the UE side. TTX_diff is the difference in chips (TTX_diff = 0, 256, …, 38144 chips) between the start of a HS-PDSCH transmission and the start of the related downlink DPCH frame. Since there are 5 possible sub-frames for the HS-PDSCH within one radio frame, TTX_diff can accordingly take one of a set of 5 possible values in a

given scenario. TTX_diff determines the transmit timing T_UlDpch-HsDpcch of the HS-DPCCH in relation to the uplink DPCH as shown in figure 5. For simplification, the parameter m = (TTX_diff/256)+101 has been introduced in specifications to express the transmit timing of the HS-DPCCH [2].

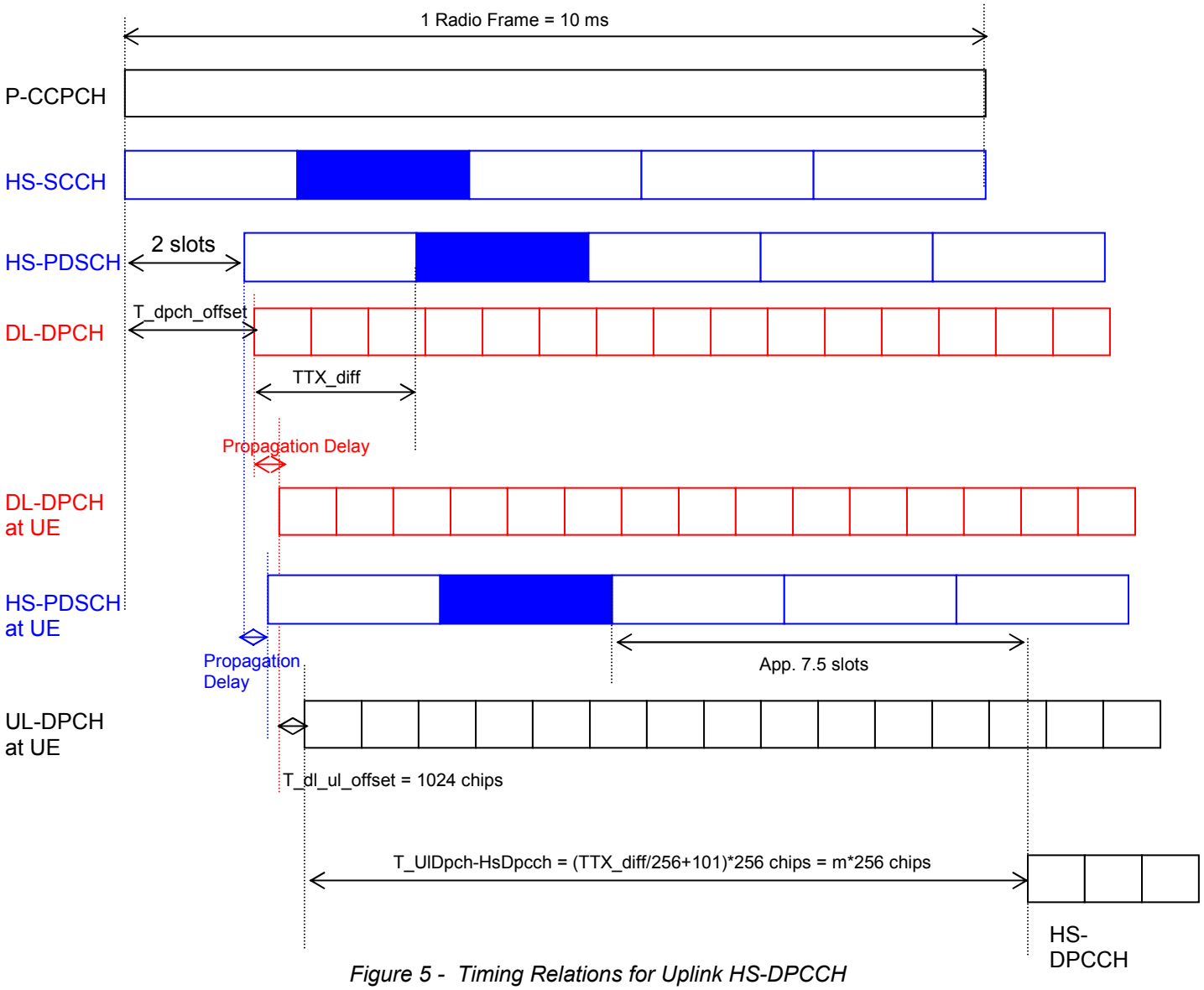

Figure 5 - Timing Relations for Uplink HS-DPCCH

The formula for m can be derived as follows:

m = TTX_diff/256 + 101 = TTX_diff/256 + (19200 chips + 3* 2560 chips - 1024 chips) / (256 chips)

It is important to remember that the setting of the DPCH frame offset (T_dpch_offset in figure 5) influences the timing of the HS-DPCCH relative to the uplink DPCCH.

Power Setting

The power of the HS-DPCCH is set in relation to the DPCCH. For this purpose, a power offset value ΔHS-DPCCH is applied by the UE on each HS-DPCCH timeslot. The UE derives this power offset from higher layer signaling as follows.

The power offset value ΔHS-DPCCH in a particular timeslot depends on whether ACK, NACK or CQI information is transmitted in this timeslot. Therefore, three different power offset values ΔACK, ΔNACK, ΔCQI are signaled by higher layers to the UE. The UE sets the power offset ΔHS-DPCCH in a particular timeslot equal to ΔACK, ΔNACK or ΔCQI, depending on what is transmitted in this timeslot.

For ΔACK, ΔNACK, ΔCQI, integer values 0…8 can be signaled by higher layers. These are then quantized in amplitude ratios according to table 1 taken from [3].

Table 1 - Quantization of power offset for HS-DPCCH

Signaling values for ΔACK, ΔNACK, ΔCQI	Quantized amplitude ratios for $10^{(\Delta_{HS\text{-}DPCCH}/20)}$
8	30/15
7	24/15
6	19/15
5	15/15
4	12/15
3	9/15
2	8/15
1	6/15
0	5/15

The gain factor βhs for non-compressed frames as referred to in figure 2 is defined in specifications as follows [4]:

$$\beta_{hs} = \beta_c \cdot 10^{\left(\frac{\Delta_{HS-DPCCH}}{20}\right)}$$

βc is the gain factor valid for the uplink DPCCH. It is either signaled by higher layers to the UE, or computed according to [4]. The same holds for the gain factor βd valid for the uplink DPDCH.

At every instant in time, at least one of the values βc and βd has the amplitude 1.0. The βc and βd values are quantized into 4 bit words. The quantization steps are given in table 2 taken from [3]:

Table 2 - Quantization of gain factors

Signaling values for β_c and β_d	Quantized amplitude ratios β_c and β_d
15	1.0
14	14/15
13	13/15
12	12/15
11	11/15
10	10/15
9	9/15
8	8/15
7	7/15
6	6/15
5	5/15
4	4/15
3	3/15
2	2/15
1	1/15
0	Switch off

The gain factors as derived by higher layer signaling are now used for scaling HS-DPCCH, DPDCH and DPCCH before transmission in the uplink, see figure 2.

In the case that the total UE transmit power after applying DPCCH power adjustments and gain factors would exceed the maximum allowed value, the UE shall apply additional scaling to the total transmit power so that it is equal to the maximum allowed power. This additional scaling shall be such that the power ratio between DPCCH and DPDCH and also DPCCH and HS-DPCCH remains as required. Any scaling shall only be applied or changed at a DPCCH slot boundary.

The maximum allowed value for UE transmit power is given in 3GPP TS 25.101 [5]. For all values of βhs the UE maximum output powers as specified in Table 3 are applicable in the case when the HS-DPCCH is fully or partially transmitted during a DPCCH timeslot. Note that table 3 is only valid for release 5. For modifications made in release 6, please refer to chapter 7.

Table 3 - UE maximum output powers with HS-DPCCH (release 5)

Ratio of β_c to β_d for all values of β_{hs}	Power Class 3		Power Class 4	
	Power (dBm)	Tol (dB)	Power (dBm)	Tol (dB)
1/15 ≤ βc/βd ≤ 12/15	+24	+1/-3	+21	+2/-2
13/15 ≤ βc/βd ≤ 15/8	+23	+2/-3	+20	+3/-2
15/7 ≤ βc/βd ≤ 15/0	+22	+3/-3	+19	+4/-2

Note that for gain factors 1/15 < βc/βd < 12/15, effectively no power reduction compared to release 99 requirements is obtained.

For gain factors 13/15 < βc/βd < 15/8, 1 dB back-off is allowed compared to release 99. For gain factors 15/7 < βc/βd < 15/0, 2 dB back-off is allowed compared to release 99.

3 Impact of HS-DPCCH on UE Power Amplifier

The HS-DPCCH as 3rd uplink code channel increases the Peak-to-Average Ratio (PAR) and therefore puts higher requirements on the linearity of UE power amplifiers. As shown in chapter 2, the standard foresees lower values for UE maximum output powers in the presence of HS-DPCCH. This was done in order to not aggravate linearity requirements on the UE power amplifiers compared to release 99. As can be seen in table 3, the UE maximum output powers depend on the gain factors, since it has been demonstrated by simulations that the required power reduction is significantly different for different combinations of βc, βd and βhs, see e.g. [6], [7], [8]. In order to avoid negative impact on uplink cell coverage, UE maximum output power reduction has only been introduced for those gain factor combinations that are most critical in terms of PAR increase.

The highest 99.9% PAR increase compared to a release 99 reference channel combination according to these simulations occurs for relations of βc/βd > 1. Besides the PAR increase, the output power probability function of the uplink signal needs to be regarded to evaluate the impact on the power amplifier. The simulations cited above have shown that in a signal with HS-DPCCH, the probability that power is above average power is much higher. Thus, the maximum output power reduction needs to be higher than the expected 99.9% PAR increase in order to meet the linearity requirements.

Obviously it is implementation dependent how a specific power amplifier copes with the linearity requirements, so it is crucial to verify the power

amplifier performance in order to meet specification requirements, e.g. Adjacent Channel Leakage Ratio (ACLR).

4 Test & Measurement Requirements

UE transmitters have to comply to test and measurement requirements as given in 3GPP specifications.

In 3GPP specification TS 34.121 [9], various new transmitter test cases for HS-DPCCH can be found:

- Test Case 5.2A: UE maximum output power with HS-DPCCH
- Test Case 5.7A: Transmit ON/OFF power, HS-DPCCH
- Test Case 5.9A: Spectrum Emission Mask with HS-DPCCH
- Test Case 5.10A: ACLR with HS-DPCCH
- Test Case 5.13.1A: Error Vector Magnitude (EVM) with HS-DPCCH

The tests are based on an uplink reference measurement channel for HS-DPCCH. β values for this reference measurement channel have already been agreed in the annex of TS 34.121 [9]. Table 4 shows the 6 sub-tests which have to be performed for each of the above-mentioned transmitter test cases with HS-DPCCH.

Table 4 - β values for transmitter characteristics tests with HS-DPCCH

Sub-test	β_c	β_d	β_c/β_d	β_{HS} (*Note1, Note 2*)
1	1/15	15/15	1/15	2/15
2	12/15	15/15	12/15	24/15
3	13/15	15/15	13/15	26/15
4	15/15	8/15	15/8	30/15
5	15/15	7/15	15/7	30/15
6	15/15	off	15/0	30/15
Note 1: Δ_{ACK}, Δ_{NACK} and Δ_{CQI} = 30/15 with β_{hs} = 30/15 * β_c .				
Note 2: For HS-DPCCH test in clause 5.7A, Δ_{CQI} = 24/15 with β_{hs} = 24/15 * β_c .				

5 Basic Test Setups with R&S Instruments

In this chapter, it is explained how to create and analyze HS-DPCCH signals for UE power amplifier testing with R&S instruments.

Generation of HS-DPCCH with R&S Instruments

For generating an HS-DPCCH signal, signal generators **SMU200A**, **SMJ100A** or **SMATE200A** are available. Software option SMx-K43 (*3GPP FDD enhanced MS/BS tests, incl. HSDPA, requires SMx-K42*) provides HSDPA functionality on these signal generators.

Alternatively, **WinIQSIM** simulation software provides the possibility to generate HS-DPCCH signals with software option SMx-K20 (*3GPP FDD incl. HSDPA*). WinIQSIM is a simulation software running on a PC to generate waveforms for digitally modulated signals which can be uploaded on the above-mentioned signal generators, on I/Q modulation generator AMIQ, or on vector signal generator SMIQ.

In the following, SMU200A signal generator and WinIQSIM simulation software are exemplarily used to demonstrate the test setup for HS-DPCCH generation.

With the SMU200A, settings for digital modulation can be accessed via the baseband function block in the block diagram of the user interface. Figure 6 shows the 3GPP FDD menu within the baseband function block. An uplink signal is created. By double-clicking on the selected User Equipment (UE1 in this example), it is possible to access more detailed settings of the generated signal including DPCCH, DPDCH, and HS-DPCCH parameters.

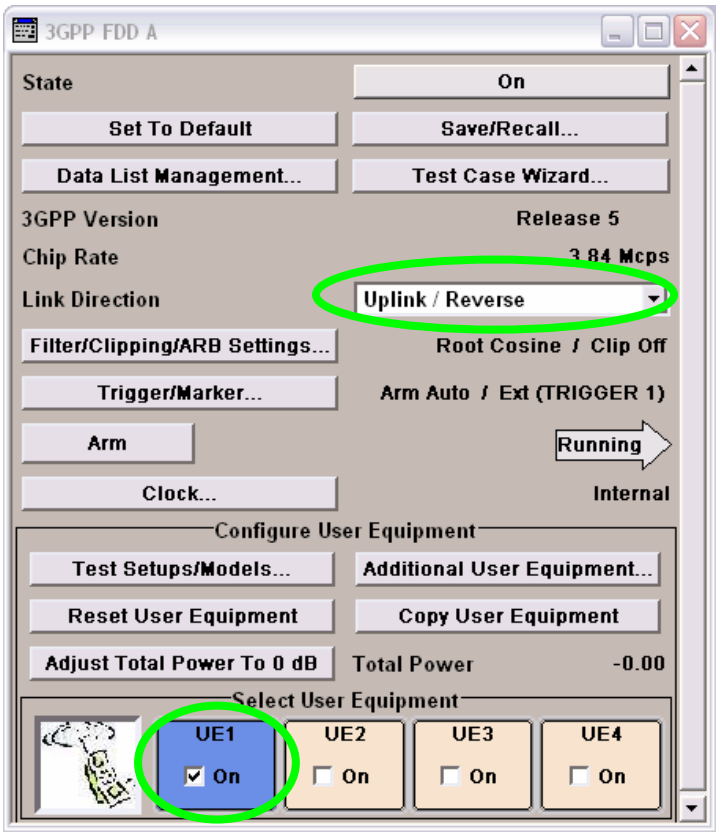

Figure 6 – Uplink signal generation with SMU200A

Figure 7 shows the corresponding menu in WinIQSIM. By double-clicking on “MS 1”, more detailed settings for HS-DPCCH, DPDCH and DPCCH can be accessed.

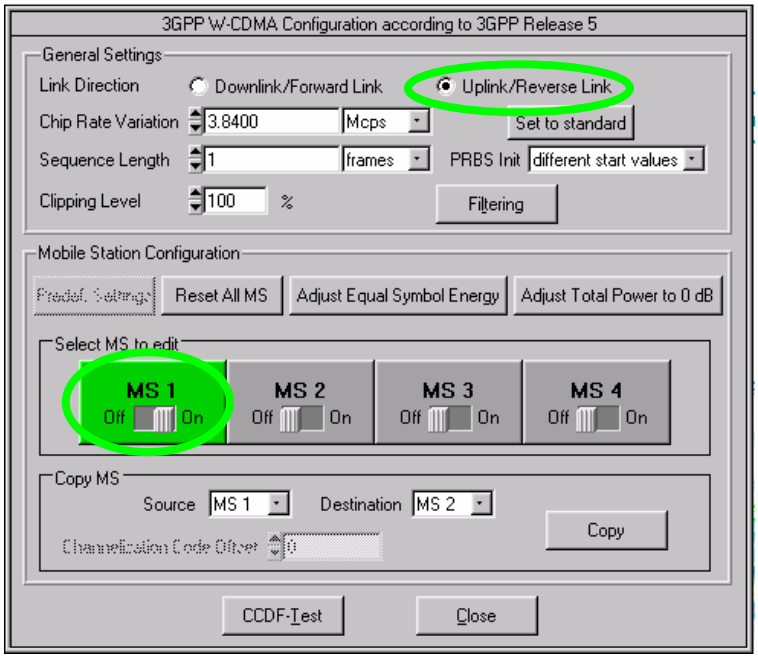

Figure 7 – Uplink signal generation with WinIQSIM

Figure 8 shows the possible HS-DPCCH settings with SMU200A. The sub-frame structure of the HS-DPCCH is graphically illustrated. Power, Start Delay, Inter TTI Distance, CQI pattern, and ACK/NACK pattern can be selected. The parameter Start Delay is corresponding to the parameter m in figure 5, and is therefore determining the position of the HS-DPCCH compared to the uplink DPCH frame boundary.

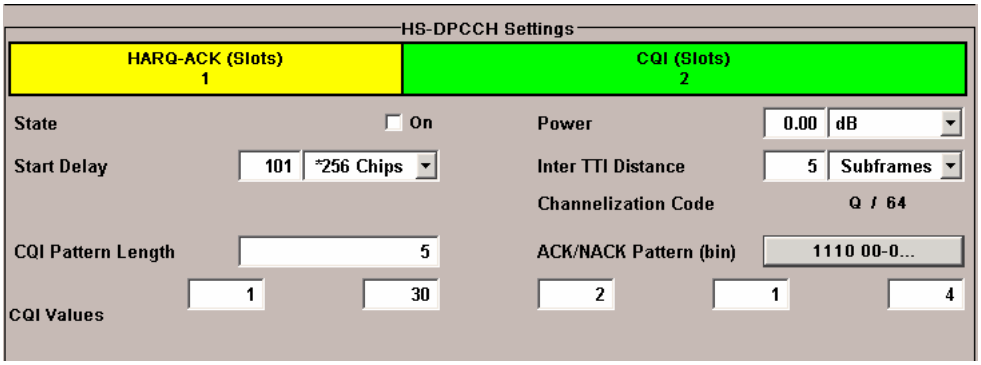

Figure 8 – HS-DPCCH Settings in SMU200A menu

With WinIQSIM, HS-DPCCH can be generated in a similar way, see figure 9. Additionally, WinIQSIM allows to set independent power values, depending on whether ACK, NACK or CQI is transmitted on HS-DPCCH. The background for this was explained in chapter 2.

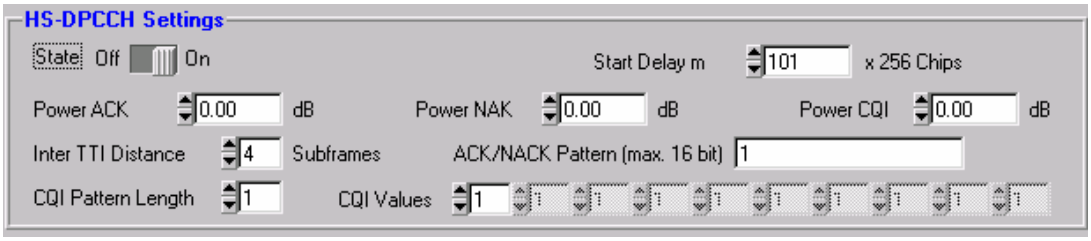

Figure 9 – HS-DPCCH Settings in WinIQSIM menu

Setting of gain factor combinations

Both in SMU200A and WinIQSIM, power of DPCCH, DPDCH and HS-DPCCH is set in dB. The power value is set in relation to the channel with the highest power. Only if **Adjust Total Power to 0 dB** is pressed in the main menu (see figure 6 and 7), the power of the individual code channels is set so that the sum power of all active channels is 0 dB. In this case, the set power differences of all channels remain the same but the total power is normalized to 0 dB.

In chapter 3, the impact of gain factor setting, i.e. setting of βc, βd, βhs, on the uplink signal characteristics was outlined. In chapter 4, it was shown

that HS-DPCCH test cases in [9] are based on sub-tests with different gain factor combinations. Therefore, it is very important to understand how to set gain factor combinations with R&S instruments.

In order to manually adjust gain factors for DPCCH and DPDCH, table 5 shows the power values to be set with the SMU200A or with WinIQSIM in order to reflect signaling values for βc and βd. Note that either βc or βd must have the signaling value 15, i.e. either DPCCH or DPDCH has to be set with level 0 dB and the level of the respective other channel is then set in relation to 0 dB according to table 5.

Table 5 – Power values to be set on SMU200A for βc and βd values

Signaling values for βc and βd	Quantized amplitude ratios for βc and βd	Power to be set for R&S Vector Signal Generator / dB
15	1.0	0.0
14	14/15	-0.60
13	13/15	-1.24
12	12/15	-1.94
11	11/15	-2.69
10	10/15	-3.52
9	9/15	-4.44
8	8/15	-5.46
7	7/15	-6.62
6	6/15	-7.96
5	5/15	-9.54
4	4/15	-11.48
3	3/15	-13.99
2	2/15	-17.52
1	1/15	-23.52
0	Switch off	Switch channel off or -80dB

In case of an additional HS-DPCCH, its level is set in relation to the DPCCH according to table 6. Note that WinIQSIM allows to set independent power values, depending on whether ACK, NACK or CQI is transmitted on HS-DPCCH.

Table 6 – HS-DPCCH power relative to DPCCH

Signaling values for Δ_{ACK}, Δ_{NACK} and Δ_{CQI}	Quantized amplitude ratios for $10^{\left(\frac{\Delta_{HS-DPCCH}}{20}\right)}$	HS-DPCCH power to be set in relation to DPCCH
8	30/15	6.02
7	24/15	4.08
6	19/15	2.05
5	15/15	0.0
4	12/15	-1.94
3	9/15	-4.44
2	8/15	-5.46
1	6/15	-7.96
0	5/15	-9.54

It needs to be considered that in the SMU200A and in WinIQSIM, the level of the channel with the highest power has to be set to 0 dB. The power of the other channels is then set in relation to 0 dB. This step is simplified with the demo software explained below in this chapter.

Analysis of HS-DPCCH with R&S Instruments

For analyzing the RF characteristics of an HS-DPCCH signal, spectrum analyzers **FSU** and **FSP** as well as the signal analyzer **FSQ** can be used. Software option FS-K73 (*Application firmware 3GPP-FDD UE transmitter test for FSMR, FSP, FSU, FSQ*) for WCDMA uplink analysis already contains the functionality required for analyzing the HS-DPCCH.

Also the **CMU200** Universal Radio Communication Tester provides a variety of analysis and measurement functions for HS-DPCCH. Software Option CMU-K64 enables HSDPA functionality. CMU200 functionality is explained at the end of this chapter.

In the following, FSQ signal analyzer is exemplarily used to demonstrate the test setup for HS-DPCCH analysis.

For power amplifier design, particularly ACLR, crest factor, EVM and spectrum measurements are of interest. These measurements can be performed conveniently and with highest accuracy with the FSQ.

For accessing the ACLR measurement, press the key MEAS, and then the ACLR softkey. The instrument measures the channel power and the relative power of adjacent channels and of the next channels. Figure 10 shows an example.

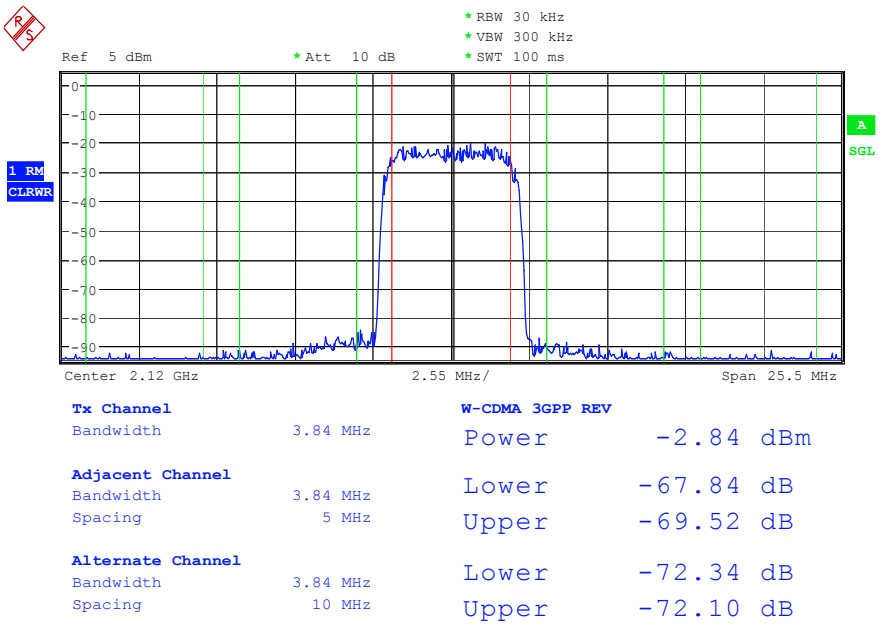

Figure 10 - ACLR measurement with FSQ

In the following you find a short explanation where you can find more relevant measurements within the FSQ menu:

- Crest factor: via key MEAS, softkey STATISTICS
- Spectrum emission mask: via key MEAS, softkey SPECTRUM EM MASK
- Composite EVM measurement: via hotkey RESULTS

Demo Software

This application note comes with a small demo program called “GDE” (Generic Demonstration Engine). The software is running on a PC. For installing it, download and start the file 1MA84_1.0.exe which will guide you through the installation process.

The GDE is a remote control command sequencer tool. It offers a user interface for setting basic parameters of an HSDPA signal with DPCCH, DPDCH, and HS-DPCCH, and for measuring ACLR, crest factor, or composite EVM of this signal. After selecting the measurement of interest and configuring the parameters, R&S instruments like SMU200A and FSQ are preconfigured via remote control, and the measurement is done automatically. Figure 11 shows the user interface of the GDE.

Within the Help menu (Help for GDE general), a detailed explanation of the software can be found.

You can select from crest factor measurement, ACLR measurement, or composite EVM measurement (1). For editing the test setup, select (2). A test editor as shown in figure 12 opens up.

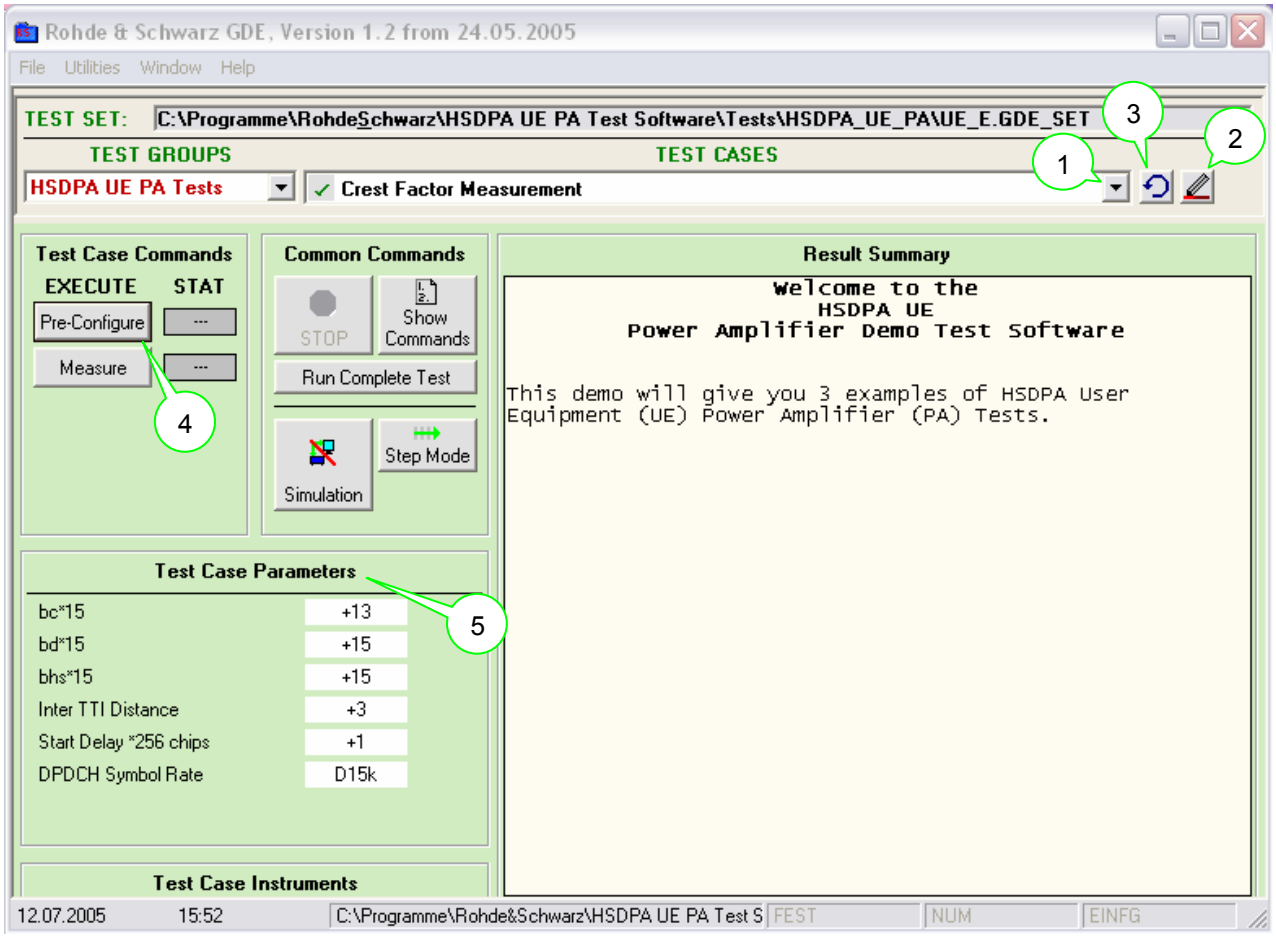

Figure 11 - User Interface of GDE, Crest Factor measurement selected

The text editor allows to input values for βc, βd and βhs (called bc, bd and bhs in this program), which are then automatically converted to the correct level setting in the SMU200A. Note that for simplicity all beta factors are assumed to be relative to the amplitude factor 1/15 in this user interface. This also reflects the gain factor settings requested for the test cases in 3GPP TS 34.121 [9]. However, for correctly determining the values, you have to be aware that the beta factor of HS-DPCCH is defined relative to the beta factor of DPCCH, see table 6. In case of no HS-DPCCH or no DPDCH signal, insert bhs = 0 or bd = 0, respectively.

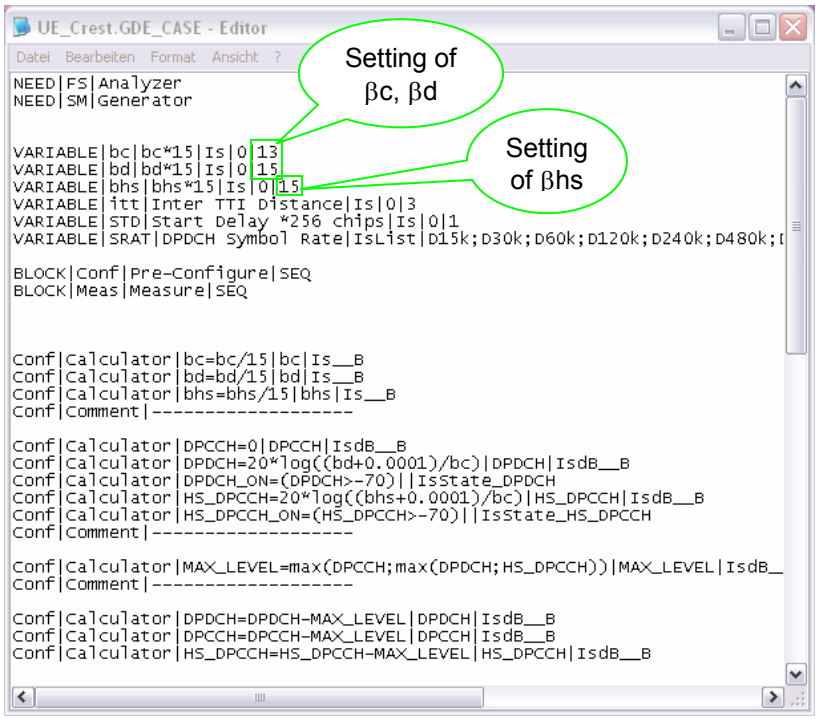

Figure 12 - Editing a test setup with the GDE

Besides beta factors, also inter TTI distance, start delay, and DPDCH symbol rate can be set. The DPDCH symbol rate can be conveniently selected in a list (figure 13).

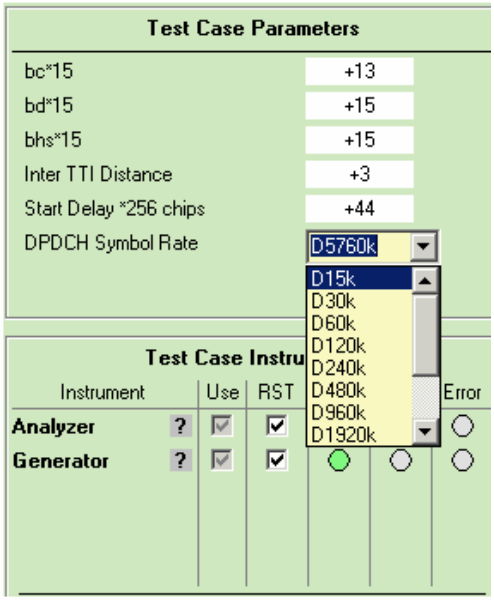

Figure 13 - User Selection of DPDCH symbol rate

The test setup file can easily be customized to enable more settings, based on the remote control commands for SMU200A and FSQ.

When you have saved your settings, reload the test setup ((3) in figure 11), pre-configure the instruments and do the measurement ((4) in figure 11). The relevant test case parameters are displayed in the user interface ((5) in figure 11).

HS-DPCCH Analysis with CMU200

The Radio Communication Tester CMU200 offers HS-DPCCH analysis functionality in signaling and non-signaling mode. In signaling mode, various parameters relevant for HS-DPCCH can be adjusted which are then signaled by higher layers (RRC – Radio Resource Control) to the UE. The UE accordingly configures its HS-DPCCH transmission. Figure 14 shows the menu where gain factors βc, βd and power offsets ΔACK, ΔNACK and ΔCQI can be set according to the signaling values as given in tables 1 and 2 of this application note.

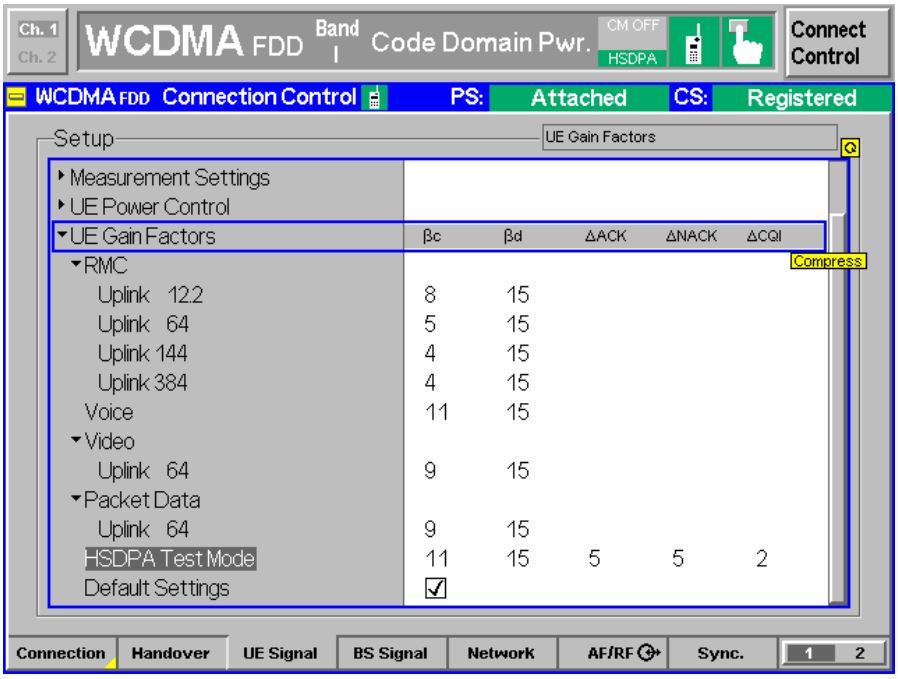

Figure 14 – Setting of gain factors in CMU200

As explained in chapter 2, the downlink DPCH frame offset (T_dpch_offset in figure 5) directly influences the timing of the HS-DPCCH in relation to the uplink DPCH frame boundary. The CMU200 allows to adjust the downlink DPCH frame offset in multiples of 256 chips which will be signaled by RRC to the UE. Figure 15 shows the menu for setting this parameter.

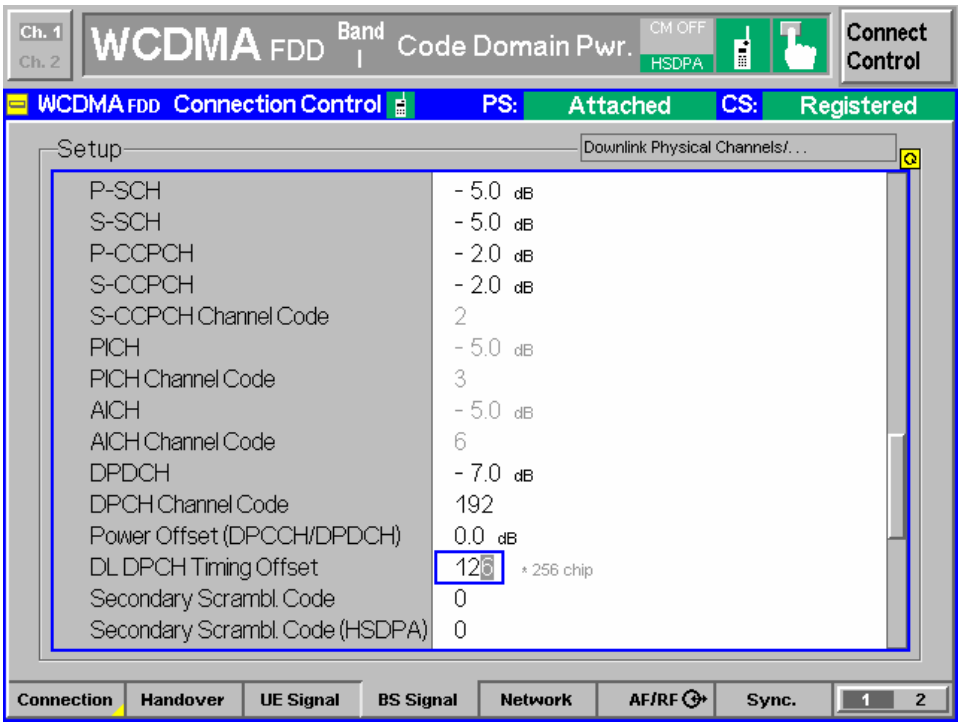

Figure 15 – Setting of Downlink DPCH frame offset in CMU200

Note that a downlink DPCH frame offset of 0 chips results in an HS-DPCCH timing of 1 symbol delay (corresponding to 1/10 of a time slot) compared to the uplink DPCH slot boundary. A downlink DPCH frame offset of 1, 11, 21, …* 256 chips will result in a slot alignment of uplink DPCH and HS-DPCCH.

Different measurement possibilities exist for the HS-DPCCH, both in signaling and non-signaling mode. An internal trigger can be generated upon HS-DPCCH reception which can be used for triggering power, spectrum, and modulation measurements. Individual trigger offsets can be adjusted. Figure 16 shows a modified code domain display which allows to estimate power levels of DPCCH, DPDCH and HS-DPCCH, as well as a representation of the power of the 10 symbols contained in one HS-DPCCH time slot. The measurement is done over one uplink DPCH time slot.

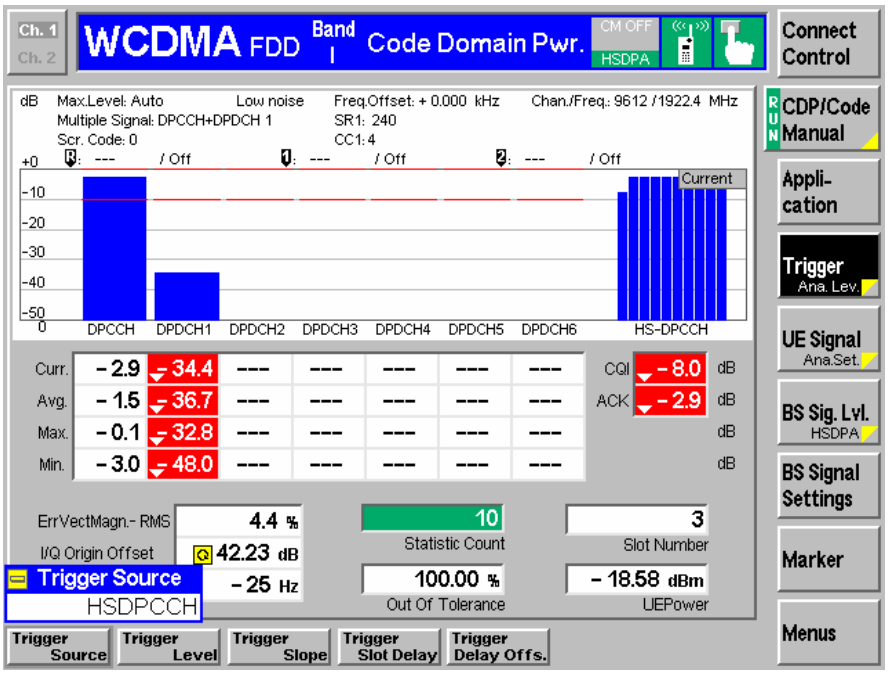

Figure 16 – Analysis of HS-DPCCH power (per symbol over a measurement interval of 1 UL DPCH time slot); HS-DPCCH with ACK/NACK and CQI

In the measurement in figure 16, HS-DPCCH is not slot aligned with uplink DPCH. The downlink DPCH frame offset is set to 0, so the HS-DPCCH time slot starts one symbol later than the uplink DPCH slot. The HS-DPCCH sub-frame in this example contains ACK/NACK and CQI values. Since different power values for ΔACK, ΔNACK and ΔCQI have been set, one can see a power step within the measured slot. Figure 17 illustrates the measurement principle

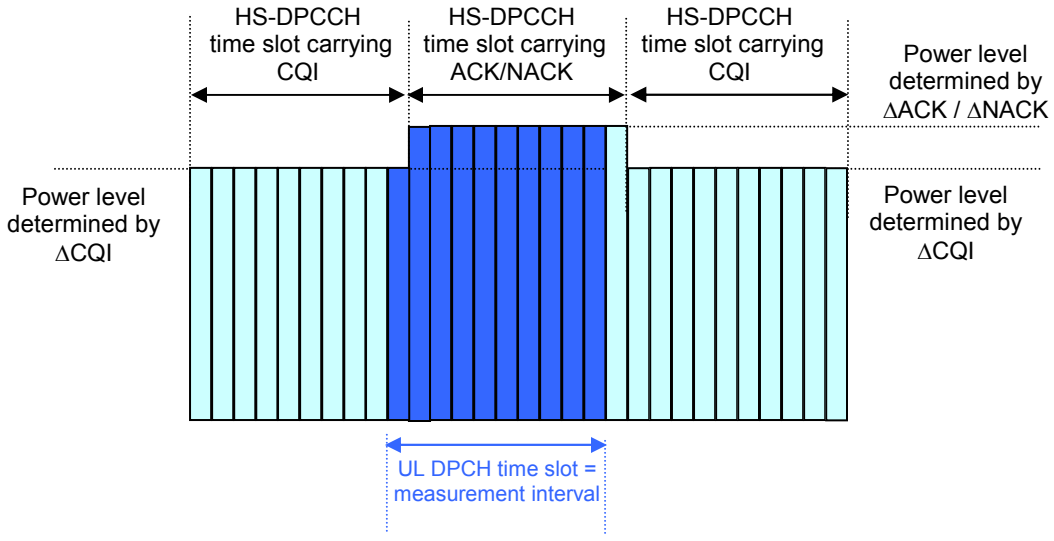

Figure 17 – HS-DPCCH slot timing not aligned with uplink DPCH slot timing

As another example, in figure 18, an HS-DPCCH sub-frame without an ACK/NACK field (DTX) has been measured.

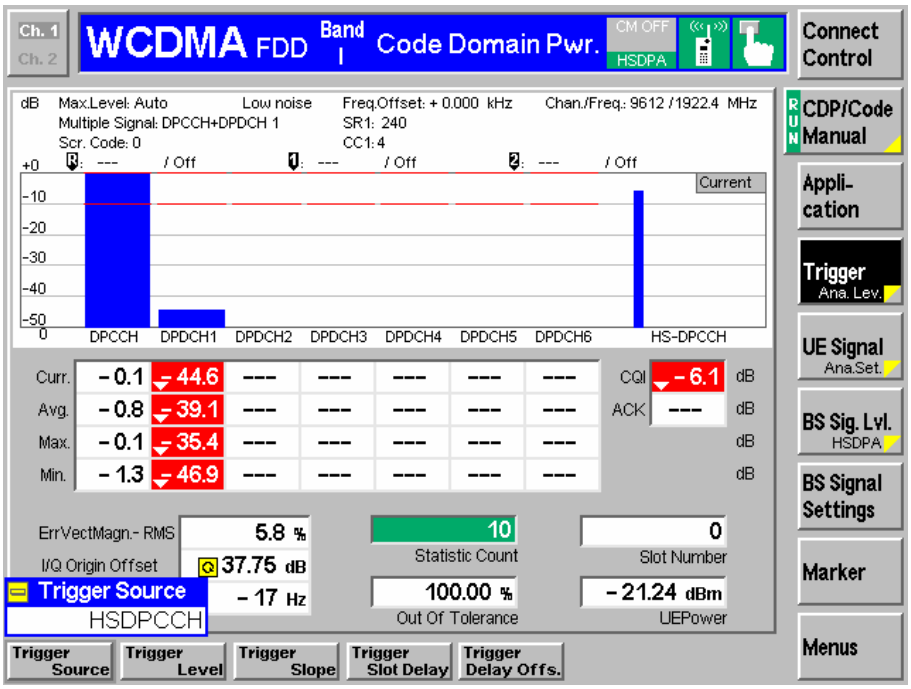

Figure 18 – Analysis of HS-DPCCH power (per symbol over a measurement interval of 1 UL DPCH time slot), no ACK/NACK field

The timing of the HS-DPCCH and the measurement interval is still as in figure 17, but this time, the ACK/NACK field of HS-DPCCH is blanked.

Figure 19 shows an EVM measurement of a signal containing HS-DPCCH.

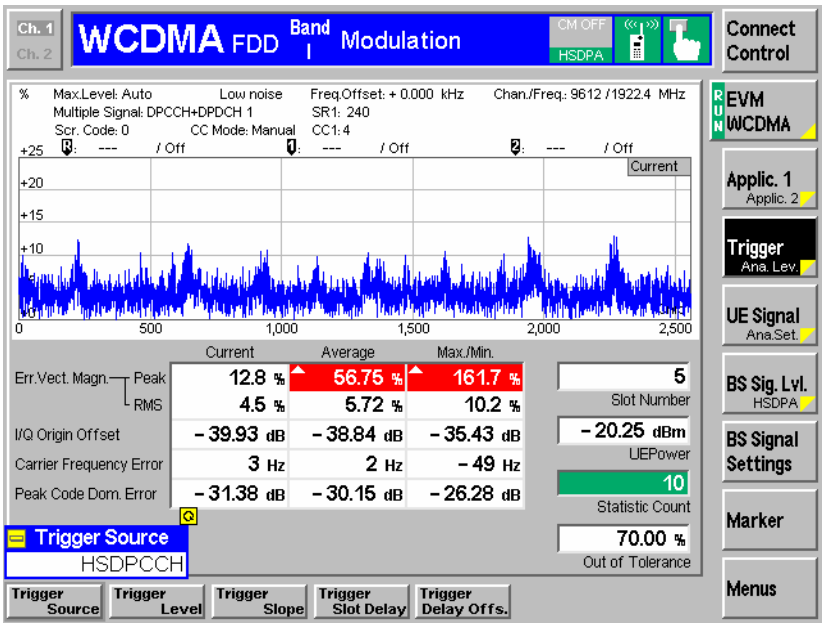

Figure 19 – EVM Measurement of a signal containing HS-DPCCH

6 Investigation of HS-DPCCH Signal Characteristics

Let us now investigate by means of some examples how the setting of gain factor combinations affects the characteristics of the HS-DPCCH signal.

Figure 20 shows the CCDF of an example reference signal without HS-DPCCH and with gain factors βc/βd = 8/15. The signal contains 1 DPDCH (channelization code 64 of SF 64). The crest factor of this signal is 3.56 dB. The measurement has been made with the FSQ.

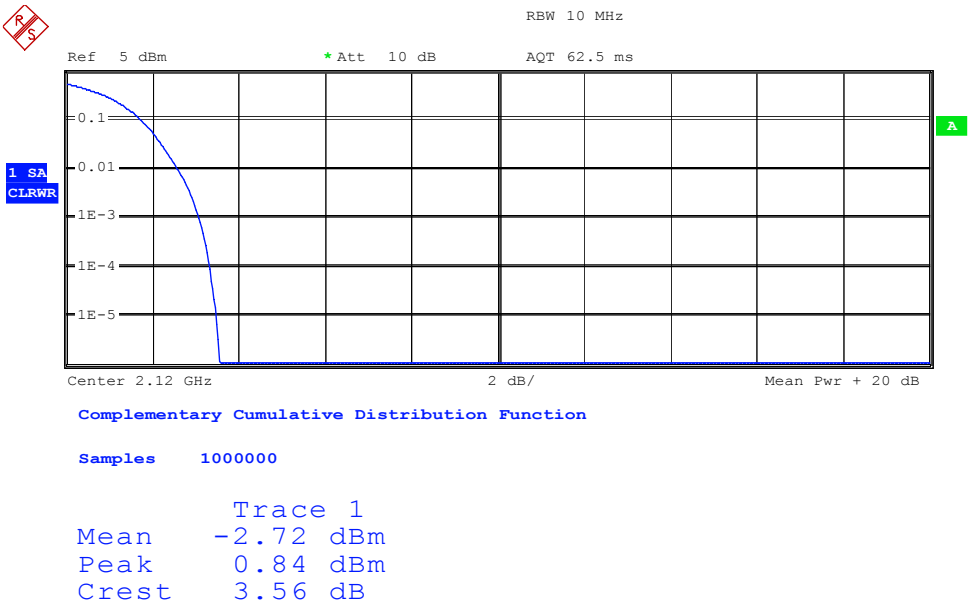

Figure 20 - Crest factor for βc/βd = 8/15, no HS-DPCCH

For comparison, an HS-DPCCH is added to this signal, and βc/βd/βhs = 15/8/15 is selected. HS-DPCCH is assumed to be time aligned to uplink DPCCH (parameter start delay = 0), and Inter TTI distance of 3 is selected.

Figure 21 shows the resulting CCDF measured with FSQ. The crest factor has increased to 6.81 dB.

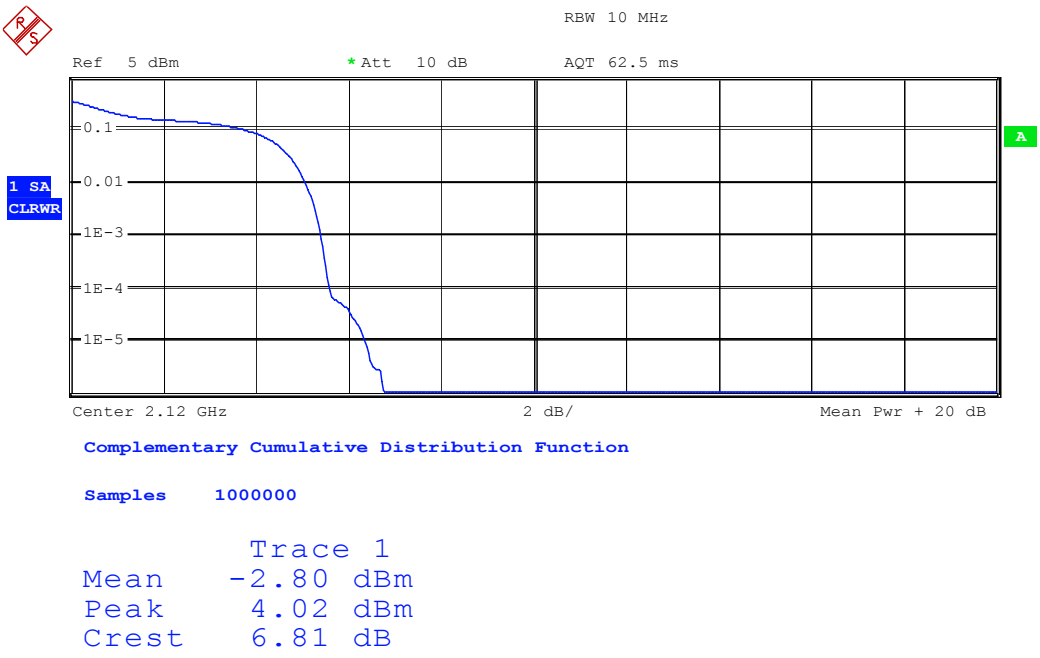

Figure 21 - Crest factor for βc/βd/βhs = 15/8/15

Obviously, the crest factor depends on a variety of parameters, and the DUT needs to be tested with a number of different configurations. It must be verified that different signal configurations are supported and specification requirements are met.

As shown in chapter 4, 3GPP TS 34.121 [9] requires to perform transmitter test cases for different gain factor combinations. In order to indicate signal characteristics for these sub-tests, the measured crest factors are listed for these signals in table 7.

Note that a DPDCH with SF 64, channelization code 64, has been chosen. Inter TTI distance is equal to 3, and start delay is equal to 0.

Table 7 - Crest Factors for different gain factor combinations

Sub-Test	*βc*	*βd*	*βhs*	*Crest Factor [dB] Inter-TTI = 1*	*Crest Factor [dB] Inter-TTI = 3*
1	1/15	15/15	2/15	3.53	3.55
2	12/15	15/15	24/15	4.58	6.87
3	13/15	15/15	26/15	4.72	7.04
4	15/15	8/15	30/15	4.86	7.94
5	15/15	7/15	30/15	4.86	7.95
6	15/15	off	30/15	3.52	6.83

7 Outlook on High Speed Uplink Packet Access

High Speed Uplink Packet Access (HSUPA) is a 3GPP release 6 feature for UMTS FDD mode, enabling uplink data rates of up to 5.76 Mbps. Main features are the introduction of an uplink scheduler in the Node B and of an Hybrid ARQ scheme for the uplink. The transmission time interval of 2 ms in uplink is introduced as UE capability; support of 10 ms transmission time interval is mandatory.

A new Enhanced Dedicated Channel (E-DCH) is introduced for HSUPA. It consists of 2 components:

- E-DPDCH (E-DCH Dedicated Physical Data Channel, SF 2…64) for carrying high speed user data
- E-DPCCH (E-DCH Dedicated Physical Control Channel, SF 256) for carrying retransmission sequence number (RSN), E-TFCI and scheduling information

Gain factors βec and βed are defined for E-DPCCH and E-DPDCH, respectively [10, 11]. They are used for weighting E-DPCCH and E-DPDCH(s) independently, see figure 22.

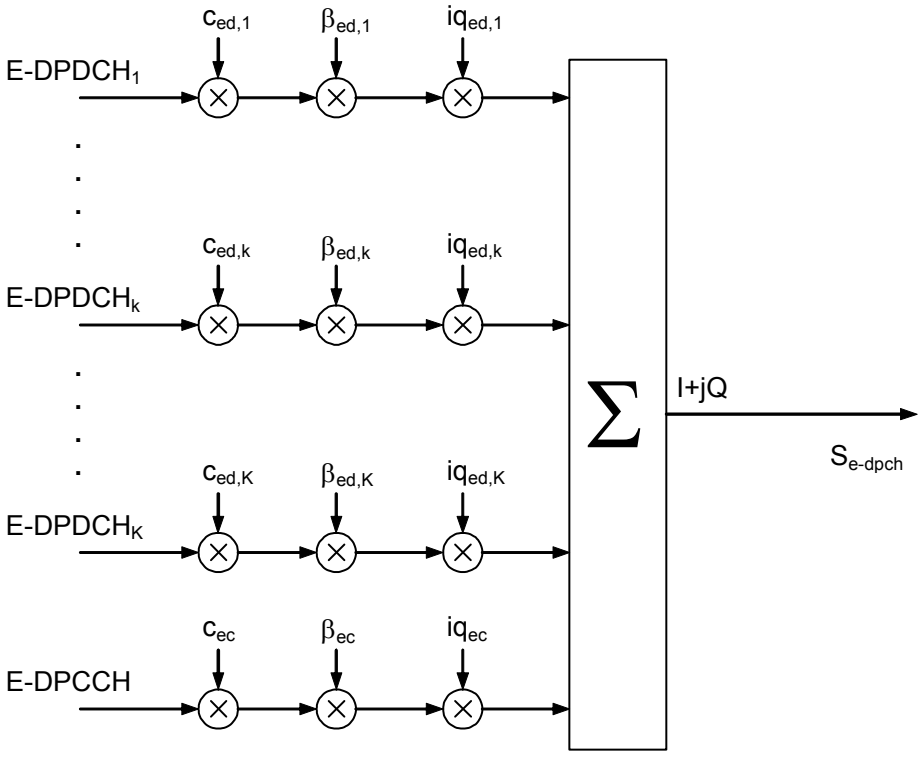

Figure 22 - Spreading for E-DPDCH / E-DPCCH

Due to these new uplink channels, PAR is increased even more compared to an HSDPA signal. Thus, HSUPA will significantly impact UE power amplifier design. Work on test specifications is currently ongoing. A new generic metric has been introduced for determining the allowed UE maximum output power reduction in the presence of HSUPA channels.

Cubic Metric

Practical experience gained in HSDPA has shown that PAR increase of a signal cannot be mapped 1-to-1 in dB to the required power back-off. With the new uplink channels in HSUPA, this issue has become even more crucial [12, 13]. Therefore, the cubic metric of a signal has been introduced in release 6 specifications as a more accurate measure for predicting the reduction in power capability of an amplifier [14]. It helps to reflect different physical channel configurations (number of codes, modulation, gain factor combinations, …).

The cubic metric (CM) is based on the UE transmit channel configuration and defined as the power of a cubed signal under test with normalized rms level relative to the power of a cubed release 99 reference signal with normalized rms level:

$$CM = [20 * \log10 ((v\_norm^3)_{rms}) - 20 * \log10 ((v\_norm\_ref^3)_{rms})] / 1.85$$

where

- v_norm is the normalized voltage waveform of the input signal
- v_norm_ref is the normalized voltage waveform of the reference signal (12.2 kbps AMR Speech)
- 1.85 is an empirical factor

Background for the cubic metric is the fact that the main cause of ACLR is the third order nonlinearity of the power amplifier's gain characteristic.

Based on the cubic metric, the maximum power reduction (MPR) for signals with HS-DPCCH and E-DCH is derived. Table 8 shows the MPR in case E-DCH or HS-DPCCH are fully or partially transmitted during a DPCCH timeslot.

Table 8 UE maximum output power with HS-DPCCH and E-DCH

UE transmit channel configuration	CM (dB)	MPR (dB)
For all combinations of; DPDCH, DPCCH, HS-DPCCH, E-DPDCH and E-DPCCH	0 ≤ CM ≤ 3.0	MAX (CM-1, 0)
Note 1: CM = 1 for β_c/β_d=12/15, β_{hs}/β_c=24/15. For all other combinations of DPDCH, DPCCH, HS-DPCCH, E-DPDCH and E-DPCCH the MPR is based on the relative CM difference. Note 2: The impact of 1 dB power control granularity is FFS.		

8 Abbreviations

3GPP	3rd Generation Partnership Project
ACK	Acknowledgement
ACLR	Adjacent Channel Leakage Ratio
AMR	Adaptive Multirate Codec
CCDF	Complementary Cumulative Distribution Function
CM	Cubic Metric
CQI	Channel Quality Indicator
DPCCH	Dedicated Physical Control Channel
DPCH	Dedicated Physical Channel
DPDCH	Dedicated Physical Data Channel
DTX	Discontinuous Transmission
DUT	Device under Test
E-DPCCH	E-DCH Dedicated Physical Control Channel
E-DCH	Enhanced Dedicated Channel
E-DPDCH	E-DCH Dedicated Physical Data Channel
E-TFCI	E-DCH Transport Format Combination Indicator
EVM	Error Vector Magnitude
FDD	Frequency Division Duplex
HARQ	Hybrid Automatic Repeat Request
HSDPA	High Speed Downlink Packet Access
HS-DPCCH	High Speed Dedicated Physical Control Channel
HS-PDSCH	High Speed Physical Downlink Shared Channel
HS-SCCH	High Speed Shared Control Channel
HSUPA	High Speed Uplink Packet Access
MPR	Maximum Power Reduction
NACK	Negative Acknowledgement
NAS	Non-Access Stratum
PAR	Peak-to-Average Ratio

P-CCPCH	Primary Common Control Physical Channel
RRC	Radio Resource Control
RSN	Retransmission Sequence Number
SF	Spreading Factor
TS	Technical Specification
TTI	Transmission Time Interval
UE	User Equipment
UMTS	Universal Mobile Telecommunications System
WCDMA	Wideband Code Division Multiple Access

9 Additional Information

This application note is updated from time to time. Please visit the website **1MA84** in order to download new versions.

Please contact TM-Applications@rsd.rohde-schwarz.com for comments and further suggestions.

10 References

[1] Application Note 1MA82; HSDPA Test and Measurement Requirements, Rohde & Schwarz

[2] 3GPP TS 25.211; Physical channels and mapping of transport channels onto physical channels (FDD) (Release 5)

[3] 3GPP TS 25.213; Spreading and Modulation (FDD) (Release 5)

[4] 3GPP TS 25.214; Physical layer procedures (FDD) (Release 5)

[5] 3GPP TS 25.101; User Equipment Radio Transmission and Reception (FDD) (Release 5)

[6] R4-030796; ACLR Requirements under HSDPA Operation, SEMC

[7] RP-040113; UE maximum power reduction when HS-DPCCH is transmitted, Nokia

[8] R4- 040102; HSDPA PA Back-off, Motorola

[9] 3GPP TS 34.121; Terminal conformance specification ; Radio transmission / reception (FDD) (Release 6)

[10] 3GPP TS 25.213; Spreading and Modulation (FDD) (Release 6)

[11] 3GPP TS 25.214; Physical layer procedures (FDD) (Release 6)

[12] R4- 040367; Comparison of PAR and Cubic Metric for Power De-rating, Motorola

[13] R4-040721; Mapping of cubic metric to additional PA headroom, Qualcomm

[14] 3GPP TS 25.101; User Equipment (UE) radio transmission and reception (FDD) (Release 6)

11 Ordering information

Vector Signal Generator

R&S® SMU200A		1141.2005.02
R&S® SMU-B102	Frequency range 100 KHz to 2.2GHz for 1st RF Path	1141.8503.02
R&S® SMU-B103	Frequency range 100 KHz to 3GHz for 1st RF Path	1141.8603.02
R&S® SMU-B104	Frequency range 100 KHz to 4GHz for 1st RF Path	1141.8703.02
R&S® SMU-B106	Frequency range 100 KHz to 6 GHz for 1st RF Path	1141.8803.02
R&S® SMU-B202	Frequency range 100 KHz to 2.2 GHz for 2nd RF Path	1141.9400.02
R&S® SMU-B203	Frequency range 100 KHz to 3 GHz for 2nd RF Path	1141.9500.02
R&S® SMU-B10	Baseband Generator with digital modulation (realtime) and ARB (64MSamples)	1141.7007.02
R&S® SMU-B11	Baseband Generator with digital modulation (realtime) and ARB (16MSamples)	1159.8411.02
R&S® SMU-B13	Baseband Main Module	1141.8003.02
R&S® SMU-K42	Digital Standard 3GPP FDD	1160.7909.02
R&S® SMU-K43	3GPP FDD Enhanced MS/BS Tests incl. HSDPA	1160.9660.02
R&S® SMU-K20	3GPP FDD incl. HSDPA for WinIQSIM	1160.9460.02
R&S® SMJ100A		1403.4507.02
R&S® SMJ-B103	Frequency range 100 kHz - 3 GHz	1403.8502.02
R&S® SMJ-B106	Frequency range 100 kHz - 6 GHz	1403.8702.02
R&S® SMJ-B10	Baseband Generator with digital modulation (realtime) and ARB (64MSamples)	1403.8902.02
R&S® SMJ-B11	Baseband Generator with digital modulation (realtime) and ARB (16MSamples)	1403.9009.02
R&S® SMJ-B13	Baseband Main Module	1403.9109.02
R&S® SMJ-K42	Digital Standard 3GPP FDD	1404.0405.02
R&S® SMJ-K43	3GPP FDD Enhanced MS/BS Tests incl. HSDPA	1404.0505.02
R&S® SMJ-K20	3GPP FDD incl. HSDPA for WinIQSIM	1404.0205.02
R&S® SMATE200A		1400.7005.02
R&S® SMATE-B103	Frequency range 100 KHz to 3 GHz for 1st RF Path	1401.1000.02
R&S® SMATE-B106	Frequency range 100 KHz to 6 GHz for 1st RF Path	1401.1200.02
R&S® SMATE-B203	Frequency range 100 KHz to 3 GHz for 2nd RF Path	1401.1400.02
R&S® SMATE-B206	Frequency range 100 kHz - 6 GHz for 2nd RF path	1401.1600.02
R&S® SMATE-B10	Baseband Generator with digital modulation (realtime) and ARB (64MSamples)	1401.2707.02
R&S® SMATE-B11	Baseband Generator with digital modulation (realtime) and ARB (16MSamples)	1401.2807.02
R&S® SMATE-B13	Baseband Main Module	1401.2907.02

R&S® SMATE-K42	Digital Standard 3GPP FDD	1404.5207.02
R&S® SMATE-K43	3GPP FDD Enhanced MS/BS Tests incl. HSDPA	1404.5307.02
R&S® SMATE-K20	3GPP FDD incl. HSDPA for WinIQSIM	1404.6603.02

Signal Analyzers, Spectrum Analyzers and Options

R&S® FSP3	9 kHz to 3 GHz	1164.4391.03
R&S® FSP7	9 kHz to 7 GHz	1164.4391.07
R&S® FSP13	9 kHz to 13 GHz	1164.4391.13
R&S® FSP30	9 kHz to 30 GHz	1164.4391.30
R&S® FSP40	9 kHz to 40 GHz	1164.4391.40
R&S® FSQ3	20 Hz to 3.6 GHz	1155.5001.03
R&S® FSQ8	20 Hz to 8 GHz	1155.5001.08
R&S® FSQ26	20 Hz to 26,5 GHz	1155.5001.26
R&S® FSQ40	20 Hz to 40 GHz	1155.5001.40
R&S® FSU3	20 Hz to 3.6 GHz	1166.1660.03
R&S® FSU8	20 Hz to 8 GHz	1166.1660.08
R&S® FSU26	20 Hz to 26.5 GHz	1166.1660.26
R&S® FSU46	20 Hz to 46 GHz	1166.1660.46
R&S® FSU50	20 Hz to 50 GHz	1166.1660.50
R&S® FS-K73	Application Firmware 3GPP-FDD UE Transmitter Test for FSMR, FSP, FSU, FSQ	1154.7252.02

Universal Radio Communication Tester (UE)

R&S® CMU200		1100.0008.02
R&S®CMU-B68var02	HW-option for CMU200 layer 1-board (3GPP/FDD, DL+UL)	1149.9809.02
R&S®CMU-B21var54	HW-option for CMU200/300: (GSM/GPRS/EDGE)	1100.5200.54
R&S® CMU-B56	HW-option for CMU200: WCDMA and data E2E for CMU-B21/var. 14	1150.1850.14
R&S® CMU-PK60	Software option for CMU200: WCDMA-Sig.: 3GPP/FDD/UE, TX-test generator, band 1+2+3+4+5+6	1159.3355.02
R&S® CMU-K64	SW-option for CMU200: HSDPA 3GPP	1157.3970.02

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